Small Size, 12-bit 1 MSPS SAR ADC

Features

- 12-Bit ADCs, no missing code
- Throughput: 1 MSPS
- INL: ±0.75 LSB
- DNL: ±0.5 LSB
- SINAD: 73 dB at 1 kHz
- THD: -85 dB at 1 kHz
- Single-ended Input Range: 0 V ~ V_{DD}
- No Pipeline Delay
- Single Supply 2.3 V ~ 5.25 V
- Packages: SOT23-6
- Standby Current: 10 nA
- Operating Temperature Range: -40 °C to +125 °C

Applications

- Precision Data Acquisition
- Automated Testing
- Precision Instrument
- Medical Instrument

General Description

ZJC2009 is low noise, low power consumption, 12-bit single-ended input SAR ADC with throughput up to 1 MSPS. The part is available in small package and easy to use. It can reduce the power consumption and complexity of the system, thus achieve high density designs.

ZJC2009 requires single power supply to sample the analog input voltage IN up to V_{DD}, which is also used as the reference voltage. Depending on V_{DD}, the ZJC2009 can be compatible with 2.5 V, 3.3 V and 5 V logic interface. The part provides one SPI-compatible serial port.

ZJC2009 is available in 6-lead SOT23 package. The operating temperature is -40 °C to +125 °C.

Typical Application

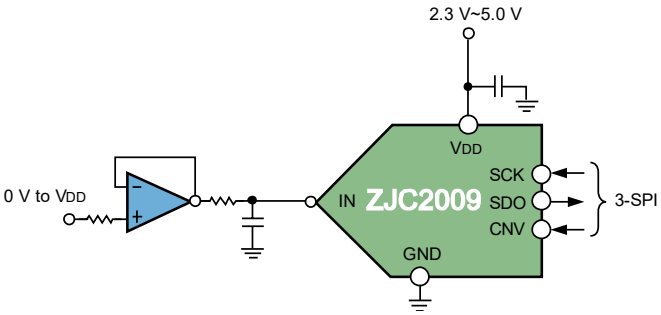


Figure 1. Application Examples

Typical Characteristics

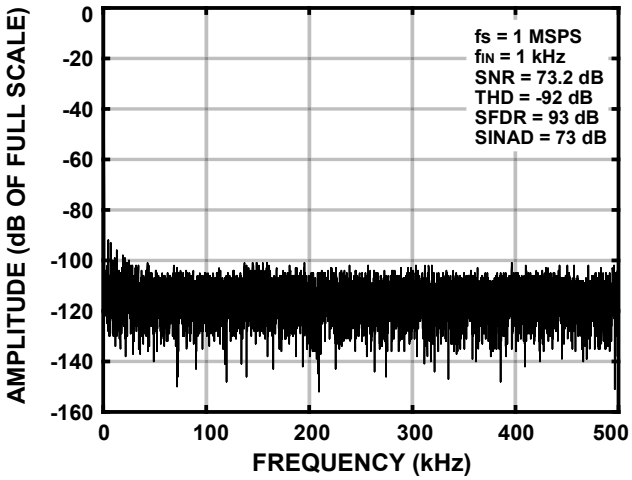


Figure 2. AC Characteristics

18/16/14/12-bit full speed SAR ADC ZJC2000 series is listed below:

Model	400 kSPS	500 kSPS	600 kSPS	1 MSPS	Packages
18-bit fully differential	ZJC2000				MSOP/DFN-10
18-bit unipolar pseudo differential	ZJC2004				
18-bit bipolar pseudo differential	ZJC2005				
16-bit fully differential		ZJC2001			
16-bit unipolar pseudo differential		ZJC2002			MSOP/DFN-10、MSOP-8
16-bit bipolar pseudo differential		ZJC2003			MSOP/DFN-10
14-bit unipolar pseudo differential			ZJC2007		MSOP/DFN-10、MSOP-8
14-bit bipolar pseudo differential			ZJC2008		MSOP/DFN-10
12-bit single-ended				ZJC2009	SOT23-6

18/16/14-bit regular speed SAR ADC ZJC2000 series are as follows:

Model	200 kSPS	250 kSPS	300 kSPS	Packages
18-bit fully differential	ZJC2010			MSOP/DFN-10
18-bit unipolar pseudo differential	ZJC2014			
18-bit bipolar pseudo differential	ZJC2015			
16-bit fully differential		ZJC2011		
16-bit unipolar pseudo differential		ZJC2012		MSOP/DFN-10、MSOP-8
16-bit bipolar pseudo differential		ZJC2013		MSOP/DFN-10
14-bit unipolar pseudo differential			ZJC2017	MSOP/DFN-10、MSOP-8
14-bit bipolar pseudo differential			ZJC2018	MSOP/DFN-10

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Version (Release B)[1]

Feb. 2025 - Release B

Updated Outline Dimensions, Related Parts

Aug. 2024

Correct Gain Error, THD, Power Consumption specifications; Update Figure 16, 17, 22.

Jun. 2024 - Release A

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Pin Configurations and Function Descriptions

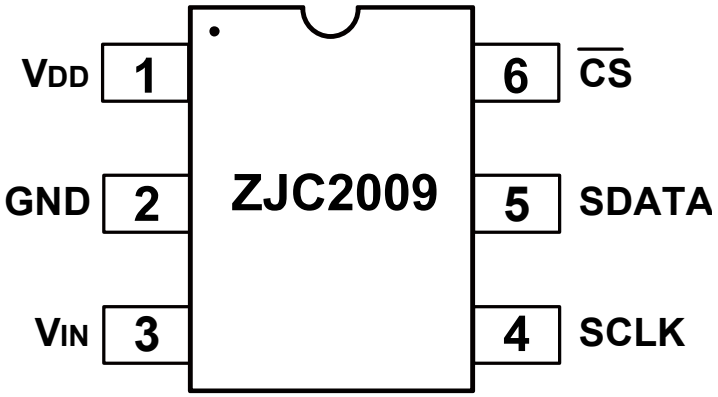


Figure 3. 6-lead SOT23 Pin Configuration

Mnemonic	Pin No.	Pin Type	Description
V_{DD}	1	Power Supply	Power Supply pin. V_{DD} ranges from 2.3 V to 5.25 V functionally. It is recommended that V_{DD} be bypassed through 100 nF and 1 nF ceramic capacitors to GND. It is also used for ADC internal reference voltage, so it should be made clean and accurate for low noise performance.
GND	2	Ground	Power Ground.
IN	3	Analog Input	Single-ended analog input channel. The input range is 0 V to V_{DD}.
SCK	4	Digital Input	Serial data clock input. SCK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the ZJC2009 conversion process
SDO	5	Digital Output	Data Out. Logic output. The conversion result is provided on this output as a serial data stream. When CNV goes low, the MSB is output on SDO. The remaining data bits are clocked out on subsequent falling edges of SCK.
CNV	6	Digital Input	Serial digital chip select input, active at low. Its rising edge is also used for conversion starting.

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Absolute Maximum Ratings [1]

Parameter	Rating
V_{DD} to GND	-0.3 V ~ 6 V
Analog Input Range	-0.3 V ~ V_{DD} + 0.3 V
Digital Input to GND	-0.3 V ~ V_{DD} + 0.3 V
Digital Output to GND	-0.3 V ~ V_{DD} + 0.3 V
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature [2]	260 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	1.5 kV
Charged Device Model (CDM) [5]	1 kV

Thermal Resistance [6]

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-6	230	76	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDECJ–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] ANSI/ESDA/JEDEC JS-002 Compliant.

[6] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

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Specifications

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, T_A = 25 °C, V_{DD} = 4.75 V ~ 5.25 V.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Resolution						12	bits
Input Characteristics							
Input Voltage		IN to GND	●	-0.1		V_{DD} + 0.1	V
Common Mode Rejection Ratio	CMRR	f_{IN} = 250 kHz			57		dB
Leakage Current		Acquisition Phase			1		nA
Input Impedance [1]							
Throughput							
Conversion Rate		V_{DD} = 5 V	●			1000	kSPS
		V_{DD} = 3.3 V	●			800	kSPS
DC Accuracy							
No Missing Codes			●	12			bits
Integral Nonlinear Error	INL		●	-1.5	±0.75	+1.5	LSB [2]
Differential Nonlinear Error	DNL		●	-0.99	±0.5	+0.99	LSB
Gain Error	GE		●	-4	±2	+4	LSB
Gain Error Temperature Drift			●		±1		ppm/°C
Zero Error	ZE		●	-0.5	±0.2	+0.5	LSB
Zero Temperature Drift					±1		ppm/°C
Power Supply Sensitivity		V_{DD} = 5 V ± 5%			±1		ppm
AC Accuracy							
Dynamic Range	DR	V_{DD} = 5 V	●	72.2	73.2		dB [3]
SNR	SNR	f_{IN} = 1 kHz, V_{DD} = 5 V	●	72	73		dB
		f_{IN} = 1 kHz, V_{DD} = 3.3 V	●	72	73		dB
Spurious-Free Dynamic Range	SFDR	f_{IN} = 1 kHz			90		dB
Total Harmonic Distortion	THD				-85		dB
Signal-to (Noise + Distortion)	SINAD	f_{IN} = 1 kHz	●	72	72.9		dB
Intermodulation Distortion	IMD	f_{IN} = 1 kHz			-90		dB
Sampling Dynamics							
-3 dB Input Bandwidth		V_{DD} = 5 V			6.5		MHz
Aperture Delay		V_{DD} = 5 V			3		ns

1 See the Analog Inputs section.
2 LSB means least significant bit. 1 LSB = 1.22 mV for 5 V input range.
3 Unless otherwise noted, all specifications expressed in decibels (dB) are referenced to full-scale input FSR and are tested with an input signal 0.5 dB below full-scale.

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Digital Input							
Logic Level	V_{IL}		•	-0.3		0.3 x V_{DD}	V
	V_{IH}		•	0.7 x V_{DD}		V_{DD} + 0.3	V
	I_{IL}		•	-1		+1	μA
	I_{IH}		•	-1		+1	μA
Digital Output							
Data Format				Serial 12-bit, Straight Binary			
Pipeline Delay				Upon the conversion is complete, the code is ready for reading			
	V_{OL}	I_{OUT} = +200 μA	•			0.4	V
	V_{OH}	I_{OUT} = 200 μA	•	V_{DD} - 0.3			V
Power Supplies							
Analog Power	V_{DD}	performance	•	4.75		5.25	V
		functional	•	2.3		5.25	V
Stand-by Current [4]		V_{DD} = 5 V	•		10	100	nA
Power Consumption		V_{DD} = 5 V, 100 kSPS throughput	•		1.7	2.1	mW
		V_{DD} = 5 V, 1 MSPS throughput	•		17	20.3	mW
		V_{DD} = 3.3 V, 800 kSPS throughput	•		6.87	8.3	mW
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		-40		+125	°C

[4] In the acquisition phase.

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Timing Specifications

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise specified, T_A = 25 °C, V_{DD} = 4.75 V ~ 5.25 V.

Parameter	Symbol		Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available (V_{DD} = 4.75 V ~ 5.25 V)	t_{CONV}	●			630	ns
Conversion Time: CNV Rising Edge to Data Available (V_{DD} ≥ 3.3 V)	t_{CONV}	●			850	ns
Acquisition Time	t_{ACQ}	●	370			ns
Time Between Conversions (V_{DD} = 4.75 V ~ 5.25 V)	t_C	●	1			µs
Time Between Conversions (V_{DD} ≥ 3.3 V)	t_C	●	1.25			µs
CNV Pulse Width	t_{CNVH}	●	10			ns
SCK Period	t_{SCK}	●	15			ns
SCK Low Time	t_{SCKL}	●	7			ns
SCK High Time	t_{SCKH}	●	7			ns
SCK Falling Edge to Data Remain Valid	t_{HSDO}	●	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}					
V_{DD} above 4.5 V		●			14	ns
V_{DD} above 3 V		●			15	ns
V_{DD} above 2.3 V		●			25	ns
CNV Low to SDO D11 MSB Valid	t_{EN}	●				
V_{DD} above 4.5 V		●			20	ns
V_{DD} above 3 V		●			22	ns
V_{DD} above 2.3 V		●			25	ns
CNV or Last SCK Falling Edge to SDO High Impedance	t_{DIS}	●			25	ns

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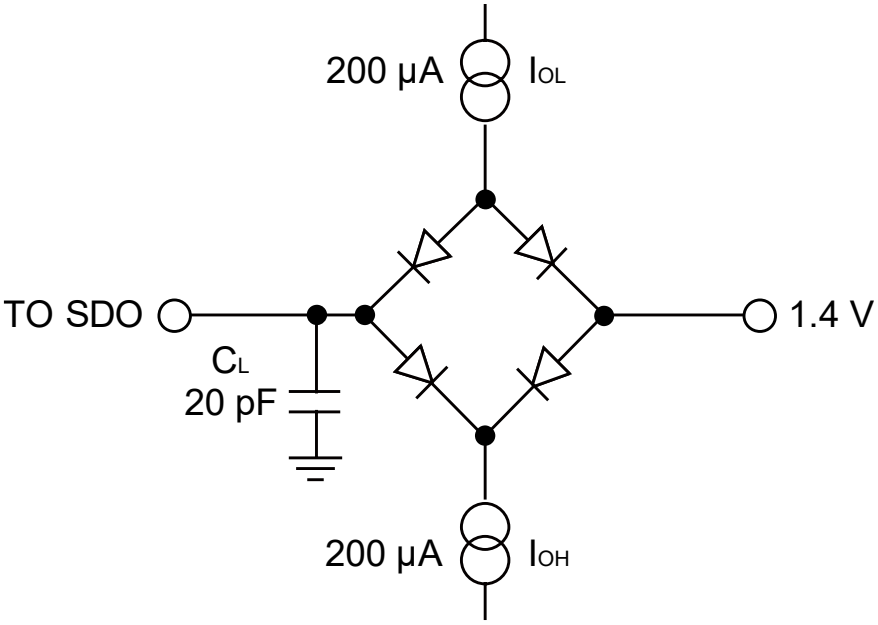


Figure 4. Load Circuit for Digital Interface Timing

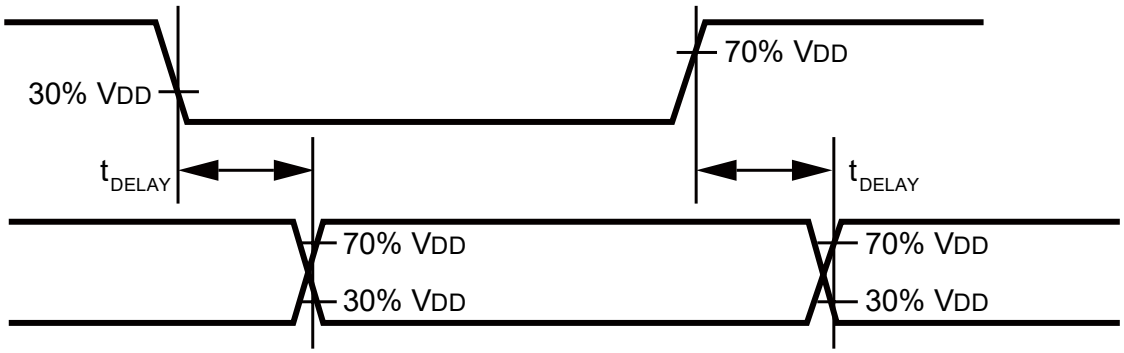


Figure 5. Voltage Levels for Digital Interface Timing

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Typical Performance Characteristics

Unless otherwise noted, V_{DD} = 5.0 V, T_A = 25 °C.

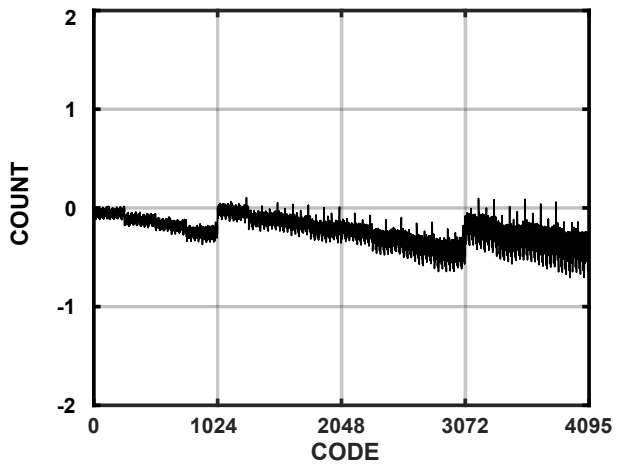


Figure 6. Integral Nonlinearity vs. Code

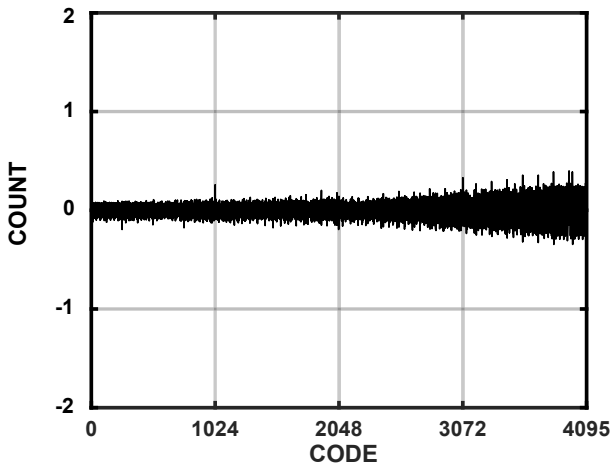


Figure 7. Differential Nonlinearity vs. Code

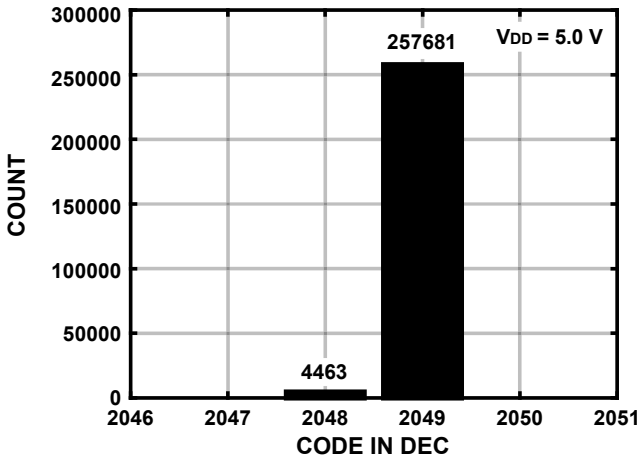


Figure 8. Histogram of DC Input (Code Center)

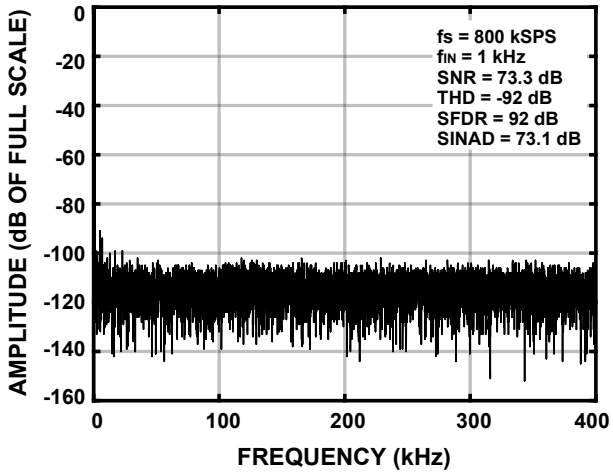


Figure 9. FFT Plot V_{DD} = 3.3 V

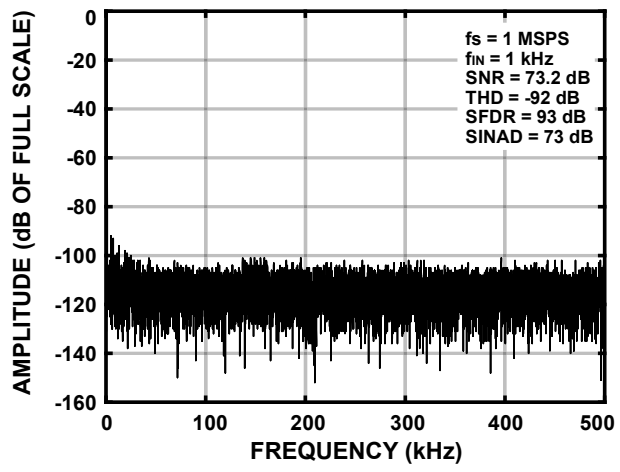


Figure 10. FFT Plot V_{DD} = 5 V

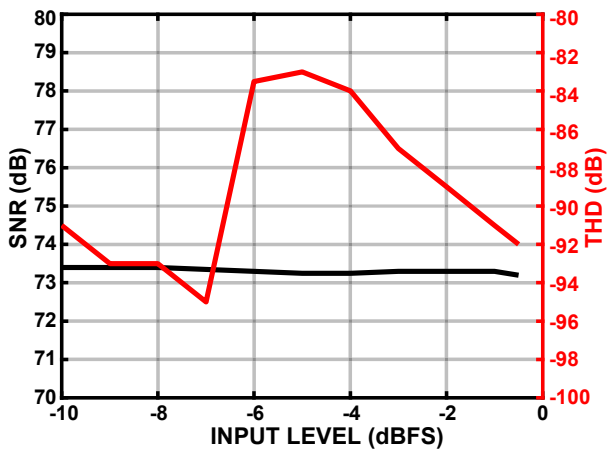


Figure 11. SNR, THD vs. Input Level

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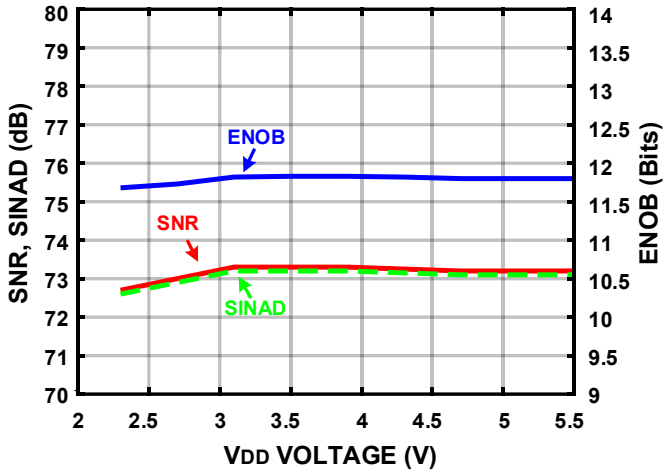


Figure 12. SINAD and ENOB vs. V_{DD} Voltage

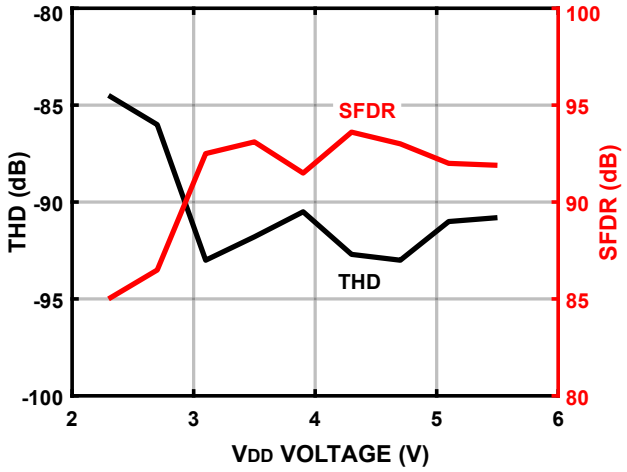


Figure 13. THD, SFDR vs. V_{DD} Voltage

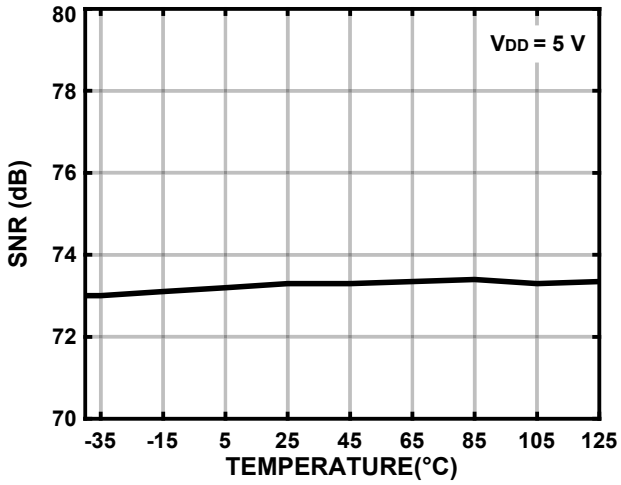


Figure 14. SNR vs. Temperature

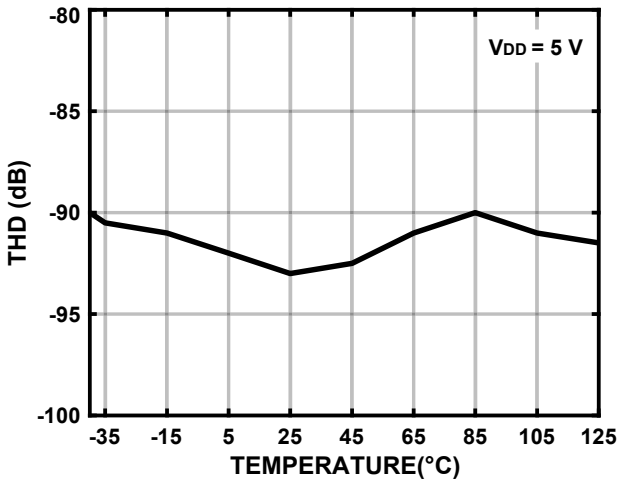


Figure 15. THD vs. Temperature

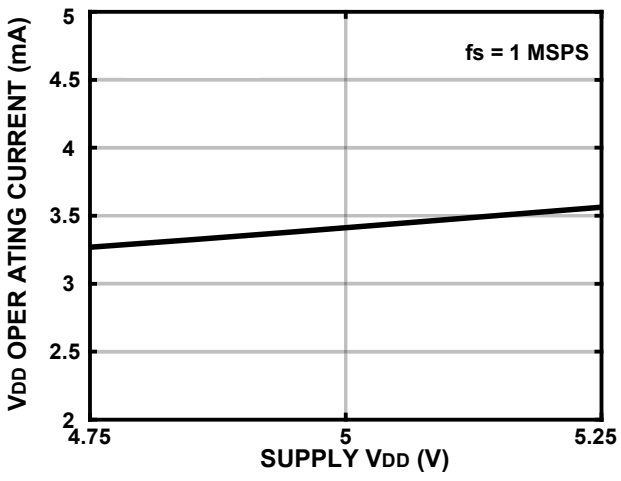


Figure 16. V_{DD} Operating Current vs. Power Supply Voltage

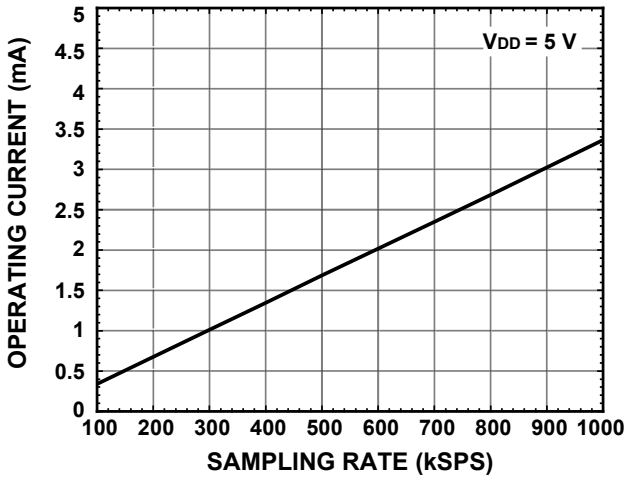


Figure 17. V_{DD} Operating Current vs. Sampling Rate

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Theory of Operation

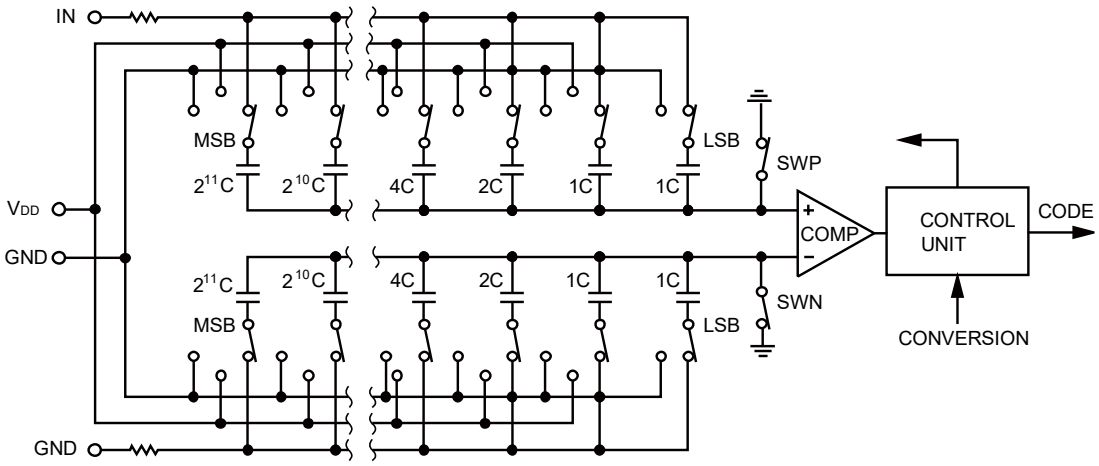


Figure 18. ADC Simplified Circuit Diagram

Circuit Structure

ZJC2009 is a fast, low power consumption, 12-bit single-ended input successive approximation analog-to-digital converter (SAR ADC). The ZJC2009 is capable of converting 1 M samples per second (1 MSPS), with the device entering stand-by mode between conversions.

The ZJC2009 can interface with 2.3 V to 5 V (V_{DD}) digital logic level and is available in a 6-lead SOT23 package which saves space.

Converter Operations

During the acquisition phase, the array node connected to the input of the comparator is short connect to GND via the SW+ and SW-. All individual switches are connected to analog inputs. Therefore, the capacitor array is used as the sampling capacitor, sampling analog signal at the IN input and GND. When the acquisition phase is complete and a rising edge occurs on the CNV input, the conversion phase is initiated. When the conversion phase begins, the SW+ and SW- disconnect first. The two capacitor arrays are then disconnected from the input and connected to the GND input. By switching the elements of the capacitor array between GND and V_{DD}, the comparator input will vary in binary weighted voltage steps ($V_{DD}/2^1$, $V_{DD}/2^2$, ..., $V_{DD}/2^{11}$). The control logic toggles these switches in sequence starting with the MSB, and the comparator is brought back into balance each time. After this process is complete, the device returns to the acquisition phase, and the control logic generates the ADC output code and busy signal indication. ZJC2009 has an on-chip conversion clock, so the conversion process does not require an external serial clock SCK.

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Transfer Function

The ideal transfer function of ZJC2009 is shown in Figure 19.

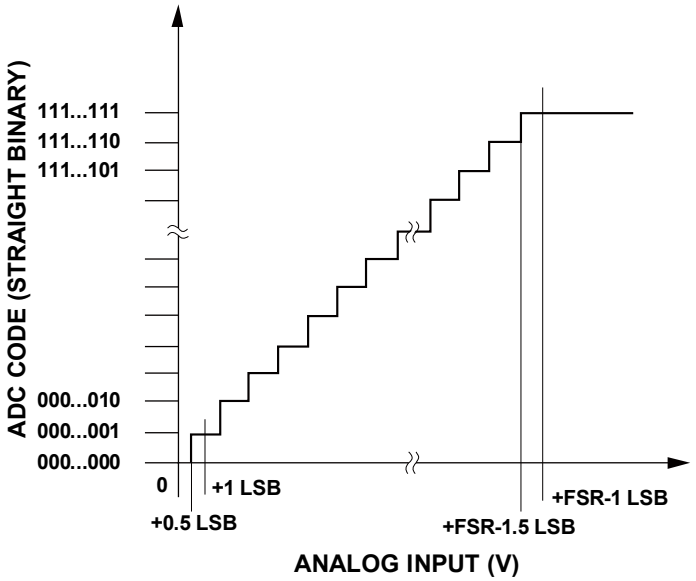


Figure 19. ADC ideal transfer function

Output Code and Ideal Input Voltage:

Description	Analog Input V_{DD} = 5 V	Digital Output (Hex)
FSR – 1 LSB	+4.99878 V	0xFFF [1]
Midscale + 1 LSB	+2.50122 V	0x801
Midscale	2.5 V	0x800
ZSR + 1 LSB	1.22 mV	0x001
ZSR	0 V	0x000 [2]

[1] This is also the code for an over-range analog input (VIN above V_{DD} – V_{GND}).
[2] This is also the code for an under-ranged analog input (VIN below V_{GND}).

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Typical Connection Diagram

Figure 20 is a suggested connection diagram for the ZJC2009.

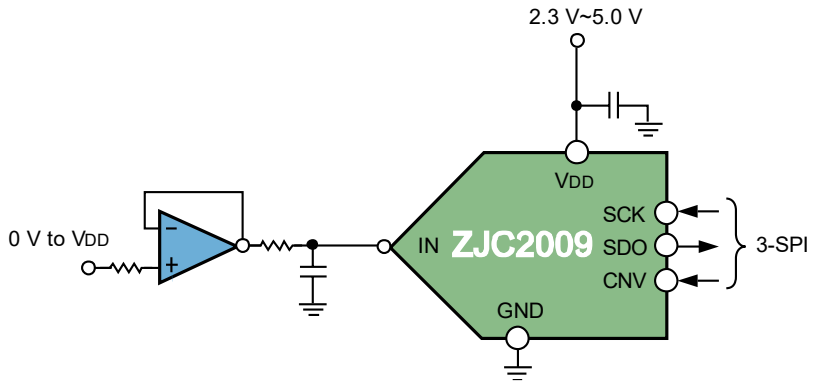


Figure 20. Typical Application Circuits

Figure 21 shows the equivalent circuit of the ZJC2009 input structure.

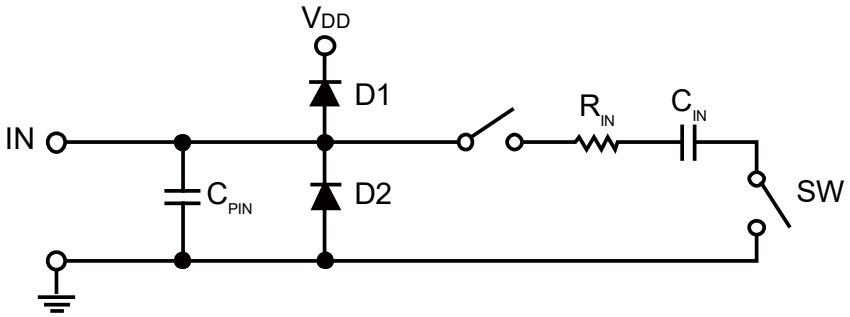


Figure 21. Two Diodes D1 and D2 Provide ESD Protection for the Analog Input

Note that the voltage of the analog input signal cannot be higher than the supply voltage (V_{DD}) by more than 0.3 V. If the voltage of the analog input signal exceeds V_{DD} + 0.3 V, the diode will be forward biased and start conducting current. These two diodes can handle forward bias currents up to 50 mA. If the supply voltage of the input driver is higher than V_{DD} the voltage of the analog input signal may be more than 0.3 V higher than the supply voltage. The two diodes D1 and D2 provide ESD protection for analog input IN+ and IN-.

During the acquisition phase, the impedance of the analog input (IN) can be seen as the parallel combination of the network formed by R_{IN} and C_{IN} in series and the capacitor C_{PIN}. C_{PIN} mainly includes pin capacitance. R_{IN} typical value is 700Ω and is a lumped element consisting of the series resistance and the on-resistance of the switch. C_{IN} typical value is 30 pF and consists mainly of the ADC sampling capacitor. High source impedance can significantly affect AC characteristics, especially harmonic distortion. THD degradation is a function of source impedance and analog input frequency.

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Power Supply

ZJC2009 uses single power supply pin V_{DD}, which can be from 2.3 V to 5 V.

The ZJC2009 automatically enters stand-by mode at the end of each conversion stage, so the power consumption is approximately linearly proportional to the sampling rate. This makes the device suitable for low sampling rate and low power consumption applications.

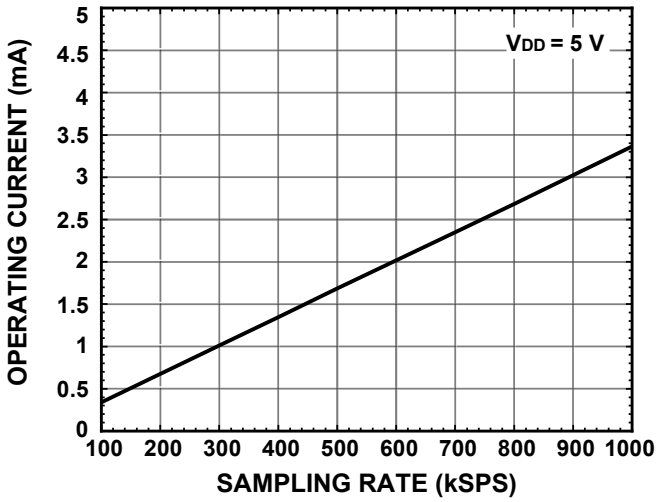


Figure 22. Operating Current vs. Sampling Rate

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Digital Interface

ZJC2009 serial interface is compatible with SPI, MCU and DSP. It uses CNV, SCK, and SDO signals.

ZJC2009 can provide the option to forcibly add a start bit before the data bits. This start bit can be used as a busy indication. If there is no busy indication, the controller must wait for the maximum conversion time before reading back the code data.

Serial Interface without Busy Indication

This mode can be used when a ZJC2009 is connected to an SPI compatible controller. The connections are shown in Figure 23 and the corresponding timing is shown in Figure 24.

A rising edge on CNV initiates a conversion, and forces SDO into a high-impedance state. Once a transition is initiated, the transition will execute to completion regardless of the state of CNV. CNV must return high before the minimum conversion time elapses and then remain high for the maximum possible conversion time to avoid generating a busy signal indication. After the conversion is completed, the ZJC2009 enters the acquisition phase and enters the stand-by mode.

When CNV goes low, the MSB is output on SDO. The remaining data bits are clocked out on subsequent falling edges of SCK. After the 12nd SCK falling edge, or when CNV goes high, whichever occurs first, SDO returns to a high-impedance state.

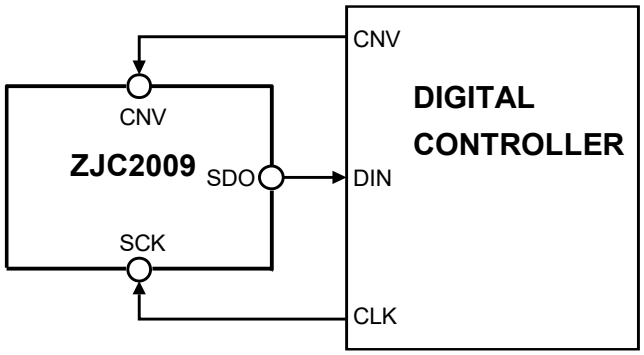


Figure 23. Serial Interface without Busy Indication Connection Diagram

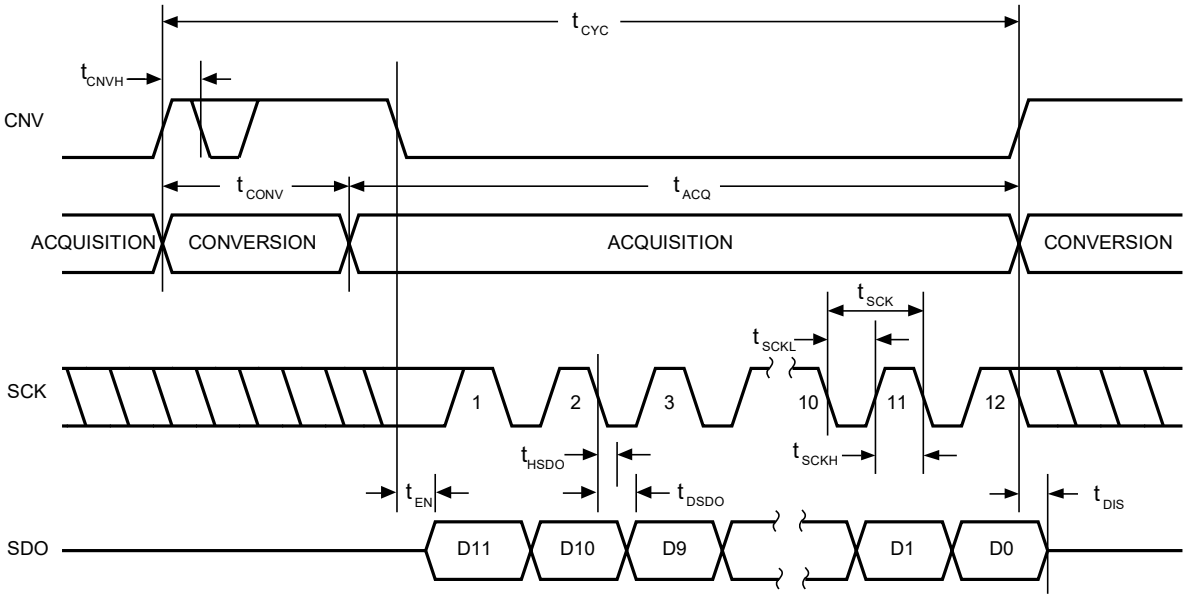


Figure 24. Serial Interface without Busy Indication Timing

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Serial Interface with Busy Indication

This mode can be used when a ZJC2009 is connected to an SPI-compatible digital host with an interrupt input. The connections are shown in Figure 25 and the corresponding timing is shown in Figure 26.

A rising edge on CNV initiates a conversion, and forces SDO into a high-impedance state. Regardless of the state of CNV, SDO remains high impedance until the conversion is complete. CNV must return to low before the minimum transition time has elapsed and then remain low for the maximum possible transition time to guarantee a busy signal indication. When the transition is complete, SDO changes from a high-impedance state to a low-impedance state. Combined with a pull-up resistor on the SDO line, this transition can be used as an interrupt signal. Next, ZJC2009 enters the acquisition stage and enters the stand-by mode. Data bits are clocked out on subsequent falling edges of SCK, MSB first. After the optional 13rd SCK falling edge, or when CNV goes high, whichever occurs first, SDO returns to a high-impedance state.

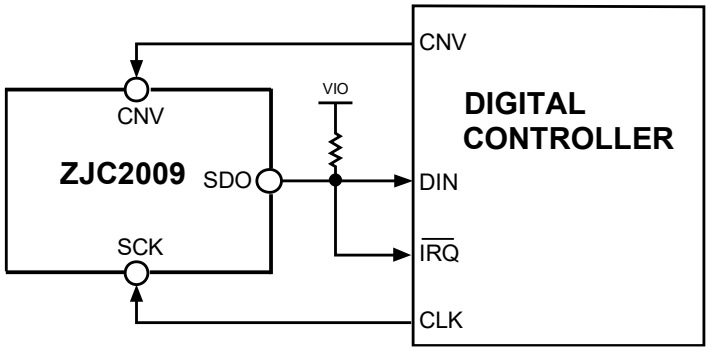


Figure 25. Serial Interface with Busy Indication Connection Diagram

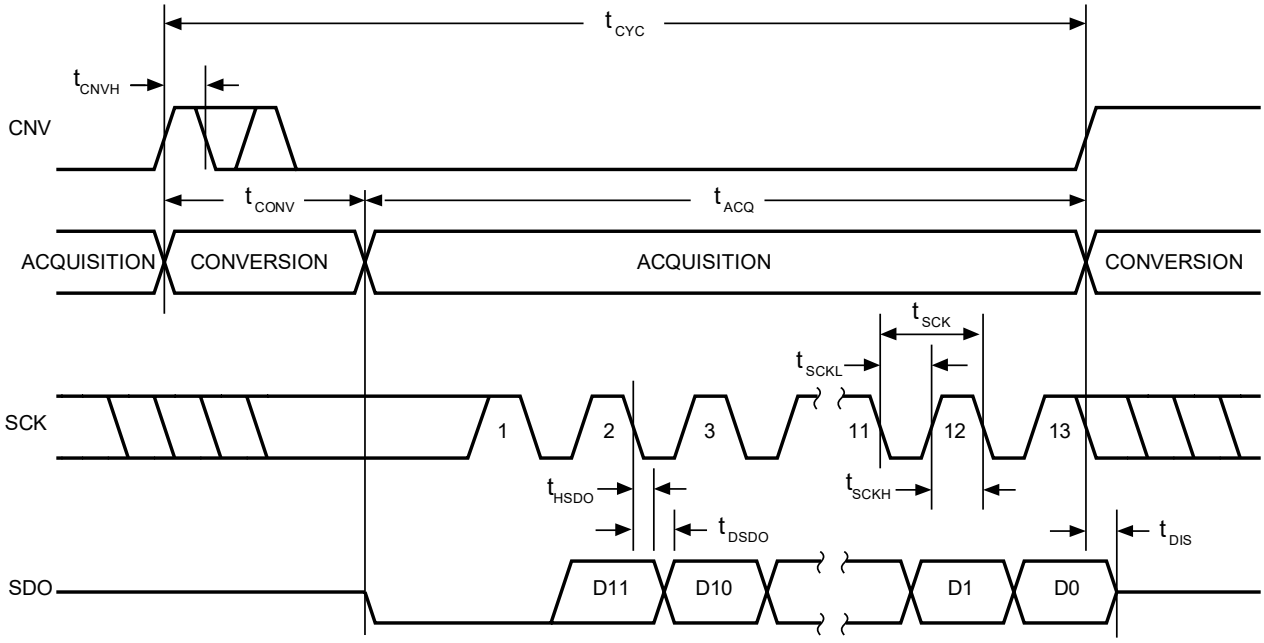


Figure 26. Serial Interface with Busy Indication Timing

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Layout Guidelines

For optimum performance of the device, good PCB layout practices are recommended, including:

- It is recommended that to use a design that separates the analog part and the digital part on the ZJC2009 PCB, and each is limited to a certain area of the circuit board.
- Avoid running digital lines under the device, which may couple noise onto the die, unless a ground plane under the ZJC2009 is used as a shield. Fast switching signals such as CNV or SCK should not be placed close to the analog signal path. Crossover of digital and analog signals should be avoided.
- At least one ground plane should be used. It can be common or split between the digital and analog sections. In the latter case, the planes should be joined close to the ZJC2009.
- The power supply V_{DD} of ZJC2009 should be decoupled with at least 100 nF and 1nF ceramic capacitors, placed close to the ZJC2009 and connected using short, wide traces to provide low impedance paths and to reduce the effect of noises on the power supply lines.

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Outline Dimensions

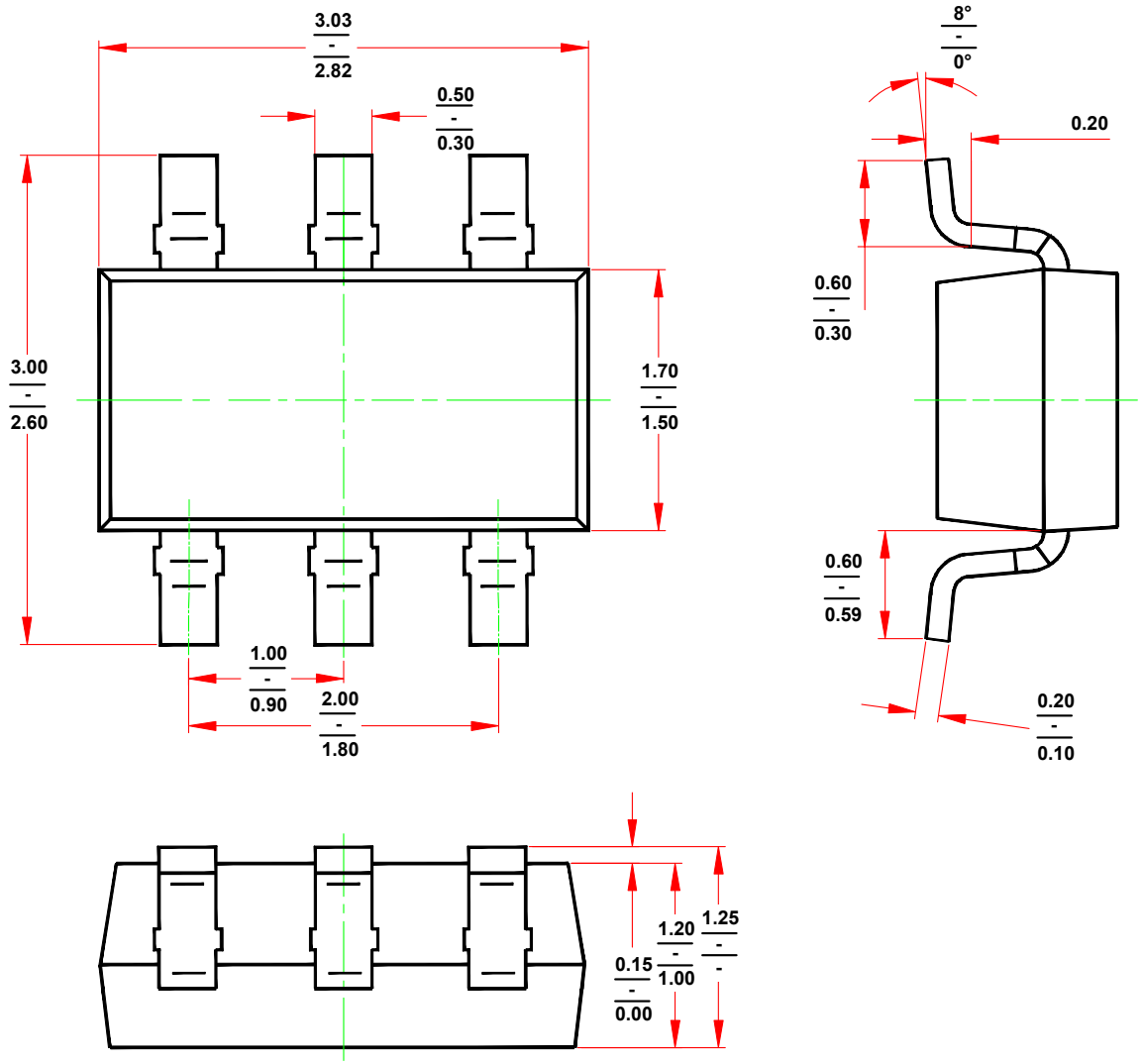


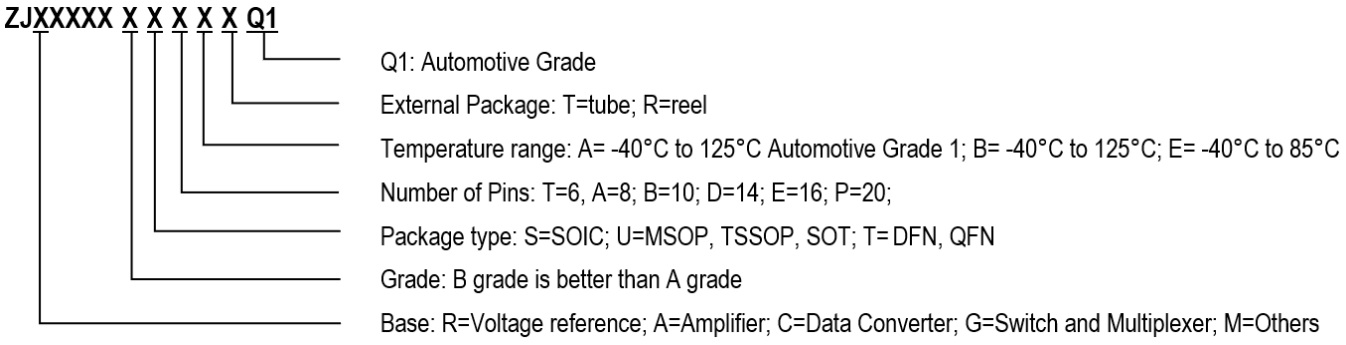
Figure 27. 6-Lead SOT23 Package Dimensions Shown in Millimeter

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Ordering Guide

Model	Orderable Device	Status[1]	Package	Resolution (bit)	Supply Voltage (V)	Temperature Range (°C)	External Package
ZJC2009	ZJC2009AUTBR	PREVIEW	SOT23-6	12	2.3 to 5.25	-40 to +125	7" Reel

Product Order Model



[1] The marketing status values are defined as follows:
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
ACTIVE: Product device recommended for new designs.
NRND: Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.
LIFEBUY: ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.
OBSOLETE: ZJW has discontinued the production of the device.

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Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN 16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G = 1 Single/Dual 36 V difference amplifier Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protectionto ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV

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